

CLAIM LISTING:

1. (Currently Amended) A circuit for decoding video data, said circuit comprising:

~~a computer readable medium storing computer executable instructions;~~

an instruction memory for storing a plurality of executable instructions;

a processor for executing the ~~computer executable plurality of executable~~ instructions, the execution of the plurality of ~~computer~~ executable instructions causing:

storing a portion of a first frame in a row of a bank of a memory; ~~and~~

storing a portion of a second frame in the same row of the same bank of the memory; and

providing a particular one of the portions of either the first frame or the second frame upon receiving a request for the particular one of the portions.

2. (Original) The circuit of claim 1, wherein the portion of the first frame and the portion of the second frame comprises a macroblock.

3. (Original) The circuit of claim 1, wherein the portion of the first frame is in a top half of the first frame, and wherein the portion of the second frame is in a top half of the second frame.

4. (Currently Amended) A circuit for decoding video data, said circuit comprising:

~~a computer readable medium storing computer executable instructions;~~

an instruction memory for storing a plurality of executable instructions;

a processor for executing the ~~computer~~ plurality of executable instructions, the execution of the ~~computer~~ plurality of executable instructions causing:

storing a top macroblock row of a first frame in a first one or more rows of memory;

storing a top macroblock row of a second frame in a second one or more rows of memory; and

providing a particular one of the macroblocks of either the first frame or the second frame upon receiving a request for the particular one of the macroblocks; and

a particular one of the first one or more rows of memory being adjacent to a particular one of the second one or more rows in the same bank of memory.

5. (Original) The circuit of claim 4, wherein the first one or more rows of memory are contiguous, and wherein the second one or more rows of memory are contiguous.

6. (Previously Presented) The circuit of claim 4, wherein execution of the plurality of instructions further causes:

storing a top macroblock row of a third frame in a third one or more rows of memory; and

wherein a particular one of the third one or more rows of memory are adjacent to another particular one of the second one or more rows of memory.

7. (Original) The circuit of claim 6, wherein execution of the plurality of instructions further causes:

storing a second macroblock row of the first frame in a fourth one or more rows of memory;

the third one or more rows of memory being continuous; and

wherein a particular one of the fourth one or more rows is adjacent to another particular one of the third one or more rows of memory.

8. (Previously Presented) A method for decoding video data, said method comprising:

storing a portion of a first frame in a row of a bank of memory; and

storing a portion of a second frame in the same row of the same bank of memory; and

providing a particular one of the portions of either the first frame or the second frame upon receiving a request for the particular one of the portions.

9. (Original) The method of claim 8, wherein the portion of the first frame and the portion of the second frame comprises a macroblock.

10. (Original) The method of claim 8, wherein the portion of the first frame is in a top half of the first frame, and wherein the portion of the second frame is in a top half of the second frame.

11. (Previously Presented) A method for decoding video data, said method comprising:

storing a top macroblock row of a first frame in a first one or more rows of memory;

storing a top macroblock row of a second frame in a second one or more rows of memory; and

providing a particular one of the macroblocks of either the first frame or the second frame upon receiving a request for the particular one of the macroblocks; and

a particular one of the first one or more rows of memory being adjacent to a particular one of the second one or more rows in the same bank of memory.

12. (Original) The method of claim 11, wherein the first one or more rows of memory are contiguous, and wherein the second one or more rows of memory are contiguous.

13. (Previously Presented) The method of claim 12, said method further comprising:

storing a top macroblock row of a third frame in a third one or more rows of memory; and

wherein a particular one of the third one or more rows of memory are adjacent to another particular one of the second one or more rows of memory.

14. (Original) The method of claim 13, further comprising:

storing a second macroblock row of the first frame in a fourth one or more rows of memory;

the third one or more rows of memory being continuous; and

wherein a particular one of the fourth one or more rows is adjacent to another particular one of the third one or more rows of memory.

15. (Cancelled)

16. (Previously Presented) The circuit of claim 1, wherein:

storing a portion of a first frame in a row of a bank of a memory further comprises storing the portion of the first frame in the row of the bank in a first memory device; and

storing a portion of a second frame in the same row of the same bank of the memory further comprises storing the portion of the first frame in the same row of the same bank of the same memory device.